UNIVERSITÀ DEGLI STUDI DI NAPOLI FEDERICO II

DOTTORATO DI RICERCA / PHD PROGRAM IN
INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

Course announcement

Title: **Design methodologies for digital circuits and systems oriented to FPGA**

Lecturer: **Gennaro Di Meo, PhD**

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Credits: **2.4**

Short Bio: Gennaro Di Meo received the M.S. degree (cum laude) in Electrical Engineering and the Ph.D degree in Information Technology and Electrical Engineering from the University of Napoli Federico II, Italy, in 2018 and 2022, respectively. Currently, he is a Researcher with the Department of Information Technology and Electrical Engineering, University of Napoli Federico II. His research interests include the design of digital VLSI circuits for telecommunication, LMS filters, and approximate computing, with particular attention to the implementation of hardware efficient multipliers for fixed-point and floating-point arithmetic. During his research activity, he has collaborated with the University of Pavia and the University of Milano Bicocca to the development of an on-chip in-band full-duplex transceiver and to the design of hardware-efficient Analog-to-Digital converters. Currently, he is collaborating with ST Microelectronics to the design of low-power floating-point arithmetic units.

Overview: In the past few decades, digital integrated circuits have occupied a central role in the realization of digital signal processing algorithms, contributing to the design of a wide range of applications in the field of Internet of Things, measurements, biomedical, and telecommunication. An efficient realization of these circuits is pivotal to meet desired hardware performance, mainly expressed in terms of power consumption. At the same time, the adoption of suitable strategies, able to lead to a cost-effective product in a short time, is also desirable to alleviate the overall effort during the design. In this context, the adoption of Field Programmable Gate Arrays (FPGA) for the implementation of digital circuits constitutes a valuable design strategy, allowing to realize circuits of medium/high complexity with reduced costs in your own lab.

The aim of the course is to give an overview of the most important strategies used to program FPGAs, with special focus to techniques for efficient complex digital systems implementation. To this end, first of all basic information will be given about the structure of FPGAs and the hardware description languages, focusing the attention on Verilog HDL. Then, the attention will be focused on the High Level Synthesis (HLS) design methodology, which exploits C-based programming languages for the design. The steps used to program the FPGA will also be presented in Vivado tool. At the end of the course, the design of hardware accelerators for practical applications will also be shown to demonstrate the potentiality of HLS design flow for FPGA.

The course will be held in English and will provide advanced computer skills (type B course).

There will be a final assessment, provided in two different modalities: students can choose to show a Power Point presentation, highlighting how FPGA can boost their own research activity, or can choose to take an oral exam on the topics covered during the course.

Schedule

Lecture	Date	Time	Room	Topics	Lecturer
1	18/02/2025	14:30-17:30	CL-T-4	Introduction to FPGA, Verilog (HDL), and design flow	G. Di Meo
2	20/02/2025	14:30-17:30	CL-T-4	High Level Synthesis (HLS) design methodology	G. Di Meo
3	25/02/2025	14:30-17:30	CL-T-4	Synthesis directives for optimal circuital architecture selection in HLS design flow	G. Di Meo
4	27/02/2025	14:30-17:30	CL-T-4	HLS-based design applications	G. Di Meo
TBD				Assessment test	

Content details

Lesson 1 – In the first part of the lesson, the inner structure of FPGA will be shown, addressing the concept of programmable connection (based on anti-fuse, SRAM, or switch MOS) and of programmable cells (LUT or MUX-based). As second step, an overview on Verilog hardware description language (HDL) will be offered, showing main statements used to describe combinatorial circuits, sequential circuits, and test bench. Then, the design flow, based on Synthesis and Place & Route steps, will be shown to translate a HDL description code into a real circuit.

Lesson 2 – In this lesson, High Level Synthesis (HLS) will be presented as an alternative way to describe digital circuits. The role of allocation, scheduling and binding phases will be addressed for the realization of digital circuits, and, focusing the attention on C/C++ languages, the correspondence between software-based code and hardware blocks will be highlighted. In the second part of the lesson, the HLS design flow will be shown using the tool Vivado. To this aim, some practical examples based on finite impulse response filtering will be discussed, able to highlight the potentiality of HLS-description approach with respect to the HDL-description approach.

Lesson 3 – In this lesson, most important synthesis directives will be discussed, which allow to realize the best suitable architecture for the target application. Specifically, the concept of loop unrolling and pipelining will be covered for the realization of hardware efficient loop-based operations (e.g. sum of products). Furthermore, directives for memory partitioning and reshaping will also be discussed, as well as the dataflow and the inline pragmas. Then, a lab session, exploiting Vivado HLS design flow, will allow to demonstrate the effects of the above directives on the final architecture of the circuit.

Lesson 4 – In the last lesson, application of HLS flow to the design of hardware accelerators used in practical scenarios will be shown, ranging from image/video processing to biomedical applications and functional system safety.

Participants are requested to join the following MS Teams group:

https://teams.microsoft.com/l/team/19%3AMLZFHATSgKaAu8b4eAyxNjNL1R1_G2ikN53i1f2tUC01%40thread.tacv2/conversations?groupId=a26ce8bc-2be5-4bb8-b8c7-33de61cd933b&tenantId=2fcfe26a-bb62-46b0-b1e3-28f9da0c45fd

One accepted in the Teams group, students have to fill the following .xlsx file with their information:

https://communitystudentiunina.sharepoint.com/:x:/s/DesignmethodologiesfordigitalcircuitsandsystemsorientedtoFPG/EVkLXsoojgZGsFsteC4s-zIBGlswCuhFle3ieKbJbux7uA?e=8U4gFb

The course is conducted on site. However, students pursuing their PhD period abroad (for research purposes) have the option to request remote attendance class via MS Teams.

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