Marco Vitone

Development of innovative techniques and methodologies for analysis and testing of Storage Systems interfaces based on System on Chip

Tutor: Prof. Nicola Petra

co-Tutor: Ing. Claudio Giaccio

Cycle: XXXVI

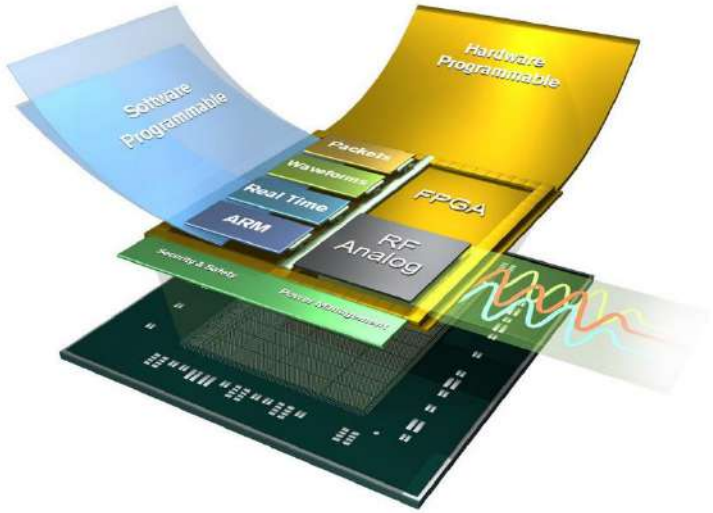
Year : 2

My background

- MSc degree in Electronics Engineering
- Research group/laboratory : VLSI Elctronics
- PhD start date : 1/11/2020
- Scholarship type: founded by Micron Semiconductor Italia S.R.L.
- Cooperation : Micron Hardware Validation Tool Team

Research field of interest

- System on Chip is a complex IC that integrates CPU, on-chip memory, programmable logic (FPGA) on a single chipset.



- My research focuses on
  - **Design** of SoC:
    - **Implementation of hardware accelerator**
    - **Validation and Debug** of SoC adopting Universal Verification Methodology (UVM)

Summary of study activities

- Ad hoc PhD courses
  - Cambridge English : Preliminary (PET)
- Courses attended borrowed from MSc curricula
  - FPGA per l'elaborazione dei segnali
- Seminar attended
  - Title :*"Introduction of Universal Verification Methodology"*
    - Lecturer : Marco Vitone
    - Place : Online Microsoft Teams, channel of MSc Course of System on Chip
    - Date : 9/11/2021

Research activity: Overview

- Convolution
  - Mono-dimensional, typical application: filters
  - Bi-dimensional, typical application: Neural Networks
  - Multi-dimensional, typical application: 3D CNN for medical applications

Research activity: Overview

- Convolution
  - Mono-dimensional, typical application: filters
  - Bi-dimensional, typical application: Neural Networks
  - Multi-dimensional, typical application: 3D CNN for medical applications
- Problem
  - Large number of multiplications
  - Hardware implementation for portability and low-power consumption

Research activity: Overview

- Objective
  - Development of Fast FIR Algorithms (FFA) for the implementation of hardware accelerators with reduced power dissipation and improved latency and throughput
  - FFAs allow using a reduced number of partial values
  - Example : mono- dimensional equations

$$y(n) = \sum_{i=0}^{k-1} x(n-i)h(i)$$

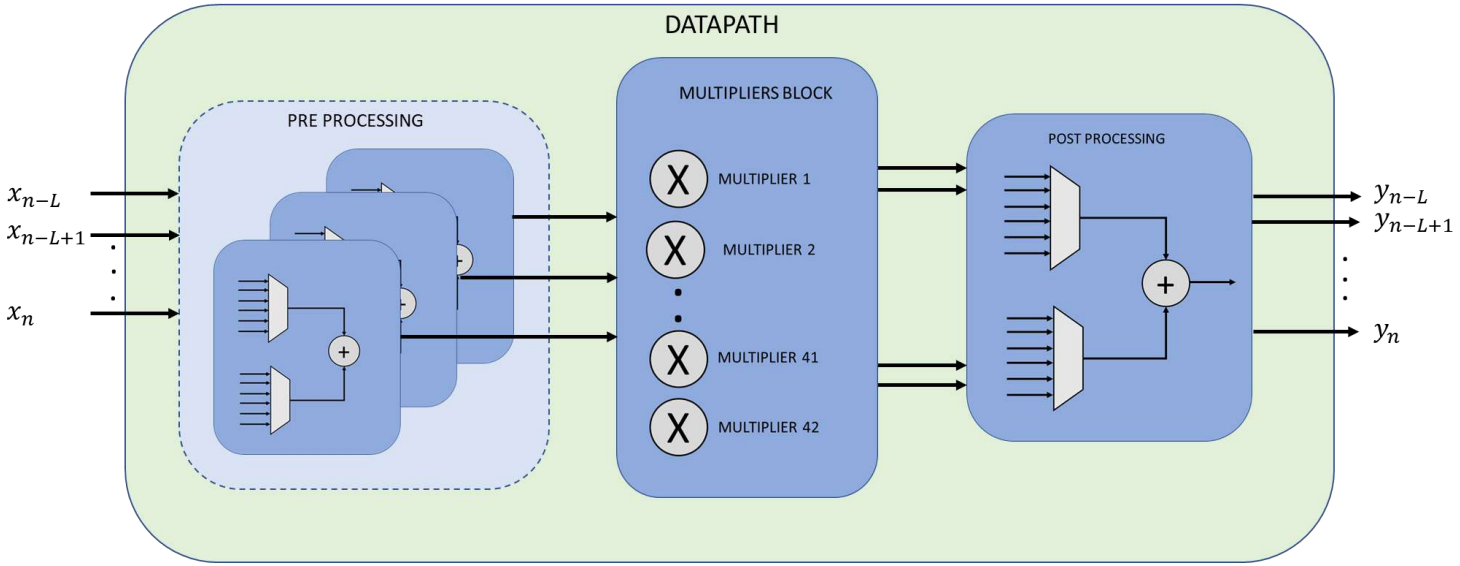
Computed by means of linear combination of partial values

$$P_1(\delta,\gamma,i) = \sum_{j1=\delta}^{\delta+\gamma-1} x((k\cdot i-1)-j1) * \sum_{j2=k-(\delta+\gamma)}^{k-\delta-1} h(j2)$$

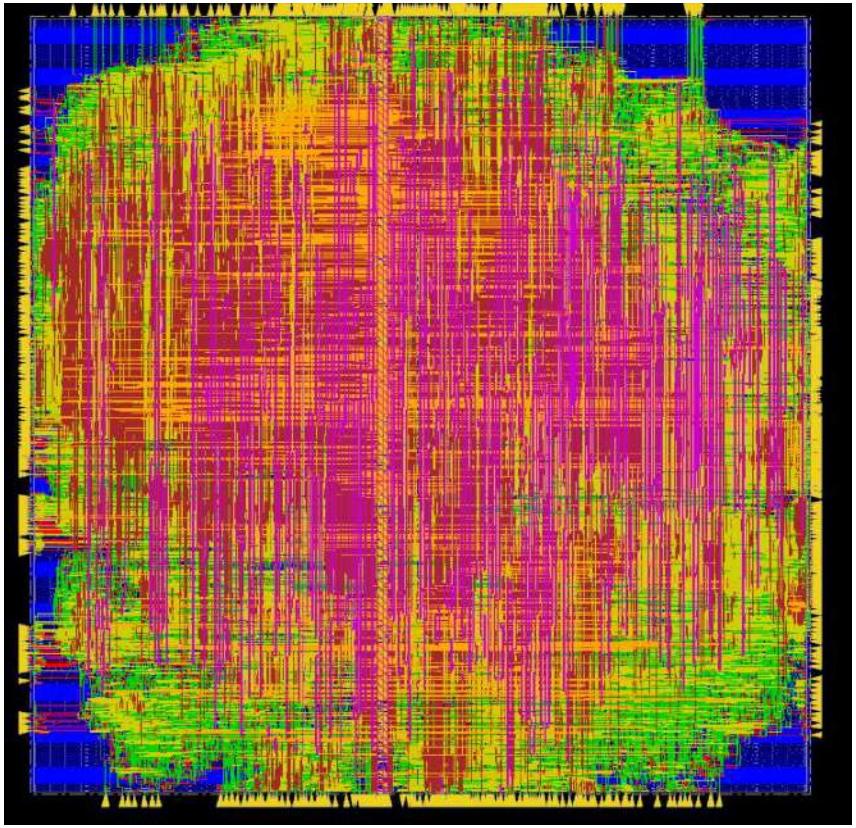
$$P_2(\delta,\gamma,i) = \left[x\big((k\cdot i-1)-\delta\big) + x\big((k\cdot i-1)-(\delta+\gamma)-1\big)\right] * \left[h\big(k-(\delta+\gamma)\big) + h(k-\delta-1)\right]$$

Accelerator Architecture

- The accelerator is optimized for neural networks
- Reference network: AlexNet
- The datapath is optimized for power and latency



Accelerator Layout



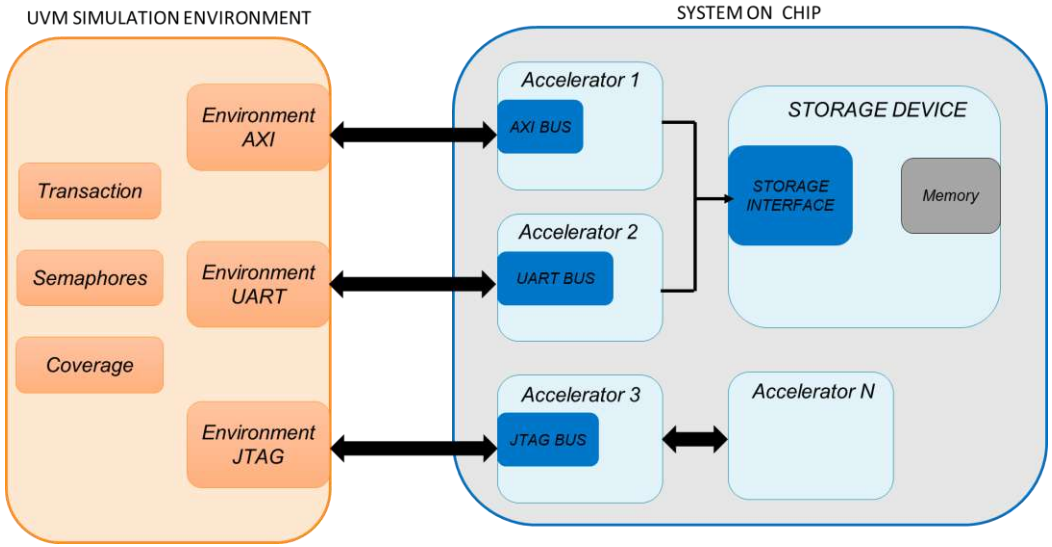
- Technology:
  - 28nm TSMC CMOS
- Area:
  - 152293 μm^2
- Power dissipation:
  - 67.5125 mW
- Frequency:
  - 500 MHz

Research activity: Overview

- Problem
  - SoC integrates a wide variety of components:
    - Processors
    - Hardware accelerator
    - Storage Interface (UFS, eMMC)
    - Bus interface (AXI, UART,JTAG and so on)
  - Thus, the validation and debug of SoC became challenging.
- Objective
  - Development of validation environments for complex SoC
  - Usage of UVM technique improving reusability, robustness and simulation coverage
  - Development of emulation environment for hardware acceleration of the validation process

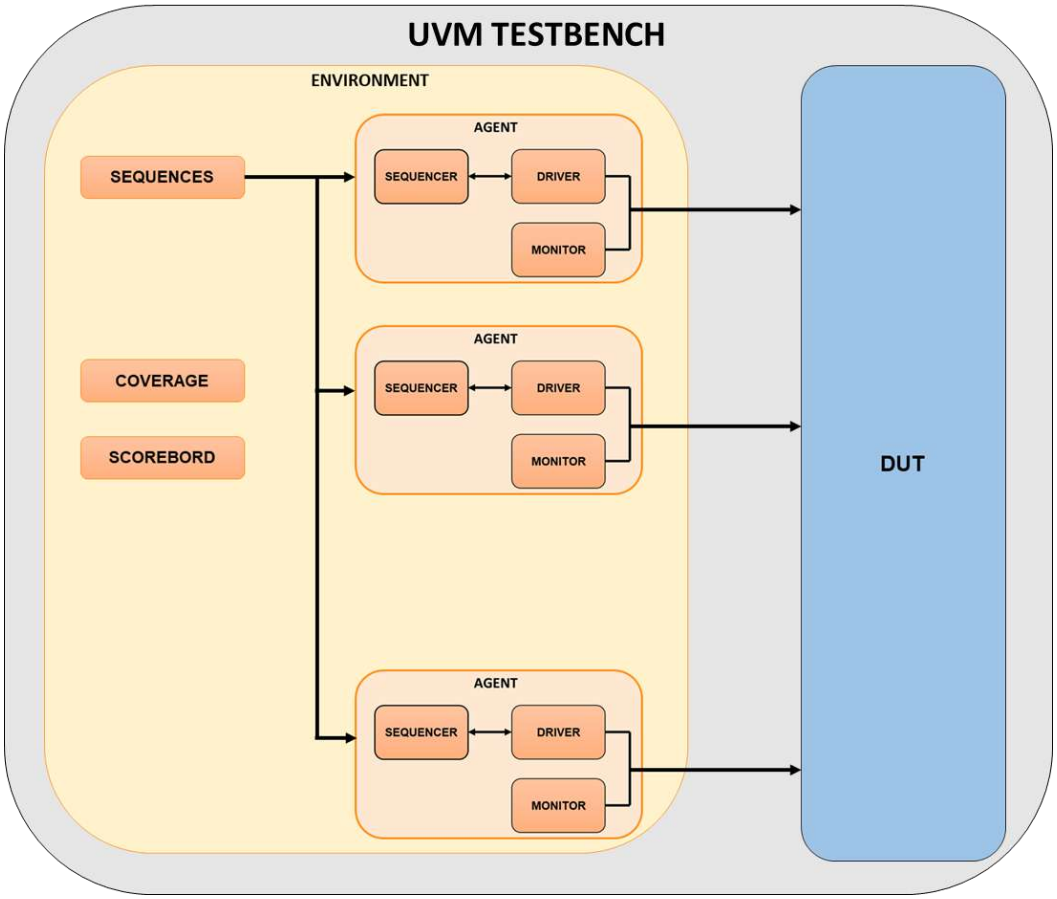
Validation Environment

- Development UVM simulation environment for a complex SoC in collaboration with Micron Team
- UVM: mixed transaction-level/pin-level modeling of system data traffic
- Goals achieved:
  - Improvement of the overall performance respect to the previous Micron custom simulation environment
  - Reduction of the simulation time : **about 50%.**
  - Improvement of the modularity, flexibility and robustness
  - Easley integration of UVM blocks from other teams/companies

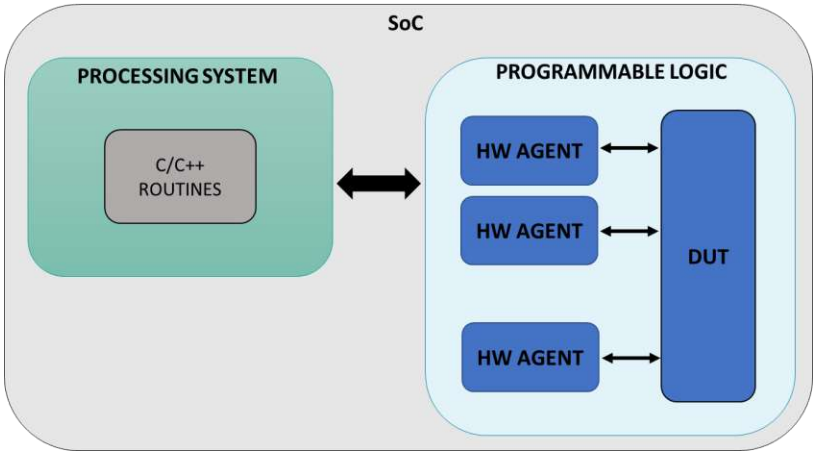


Emulation Environment

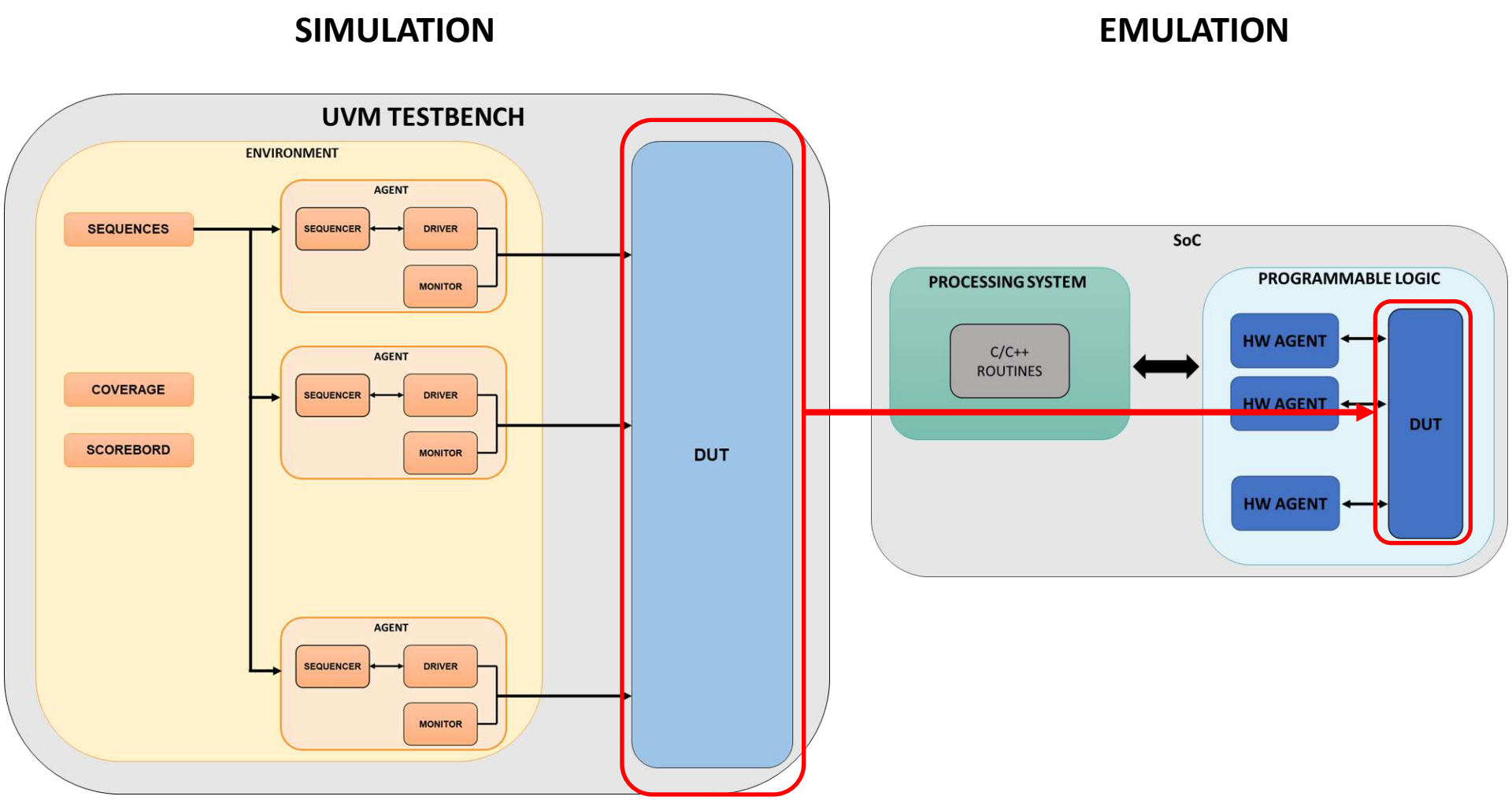
SIMULATION



EMULATION



Emulation Environment



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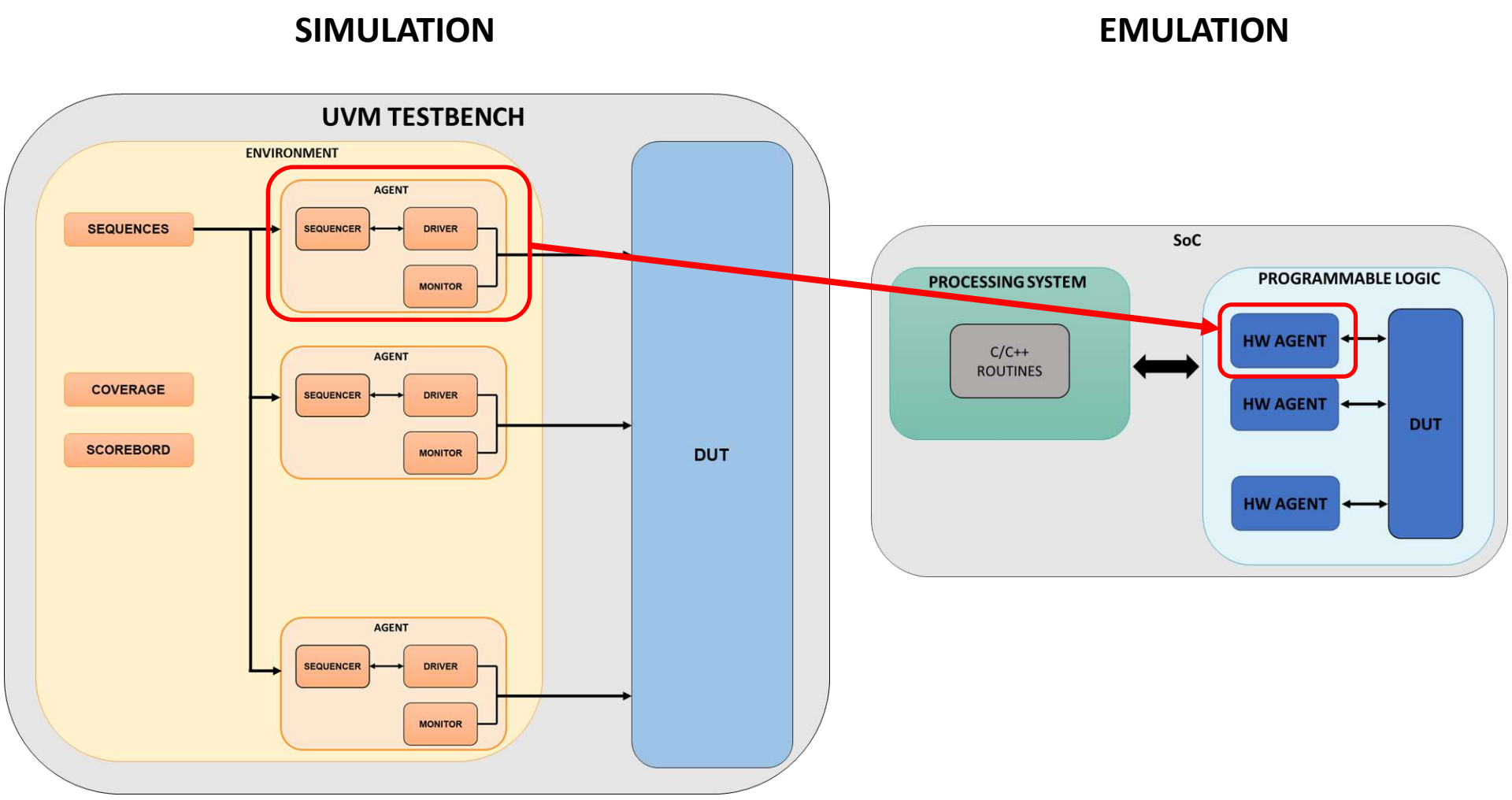

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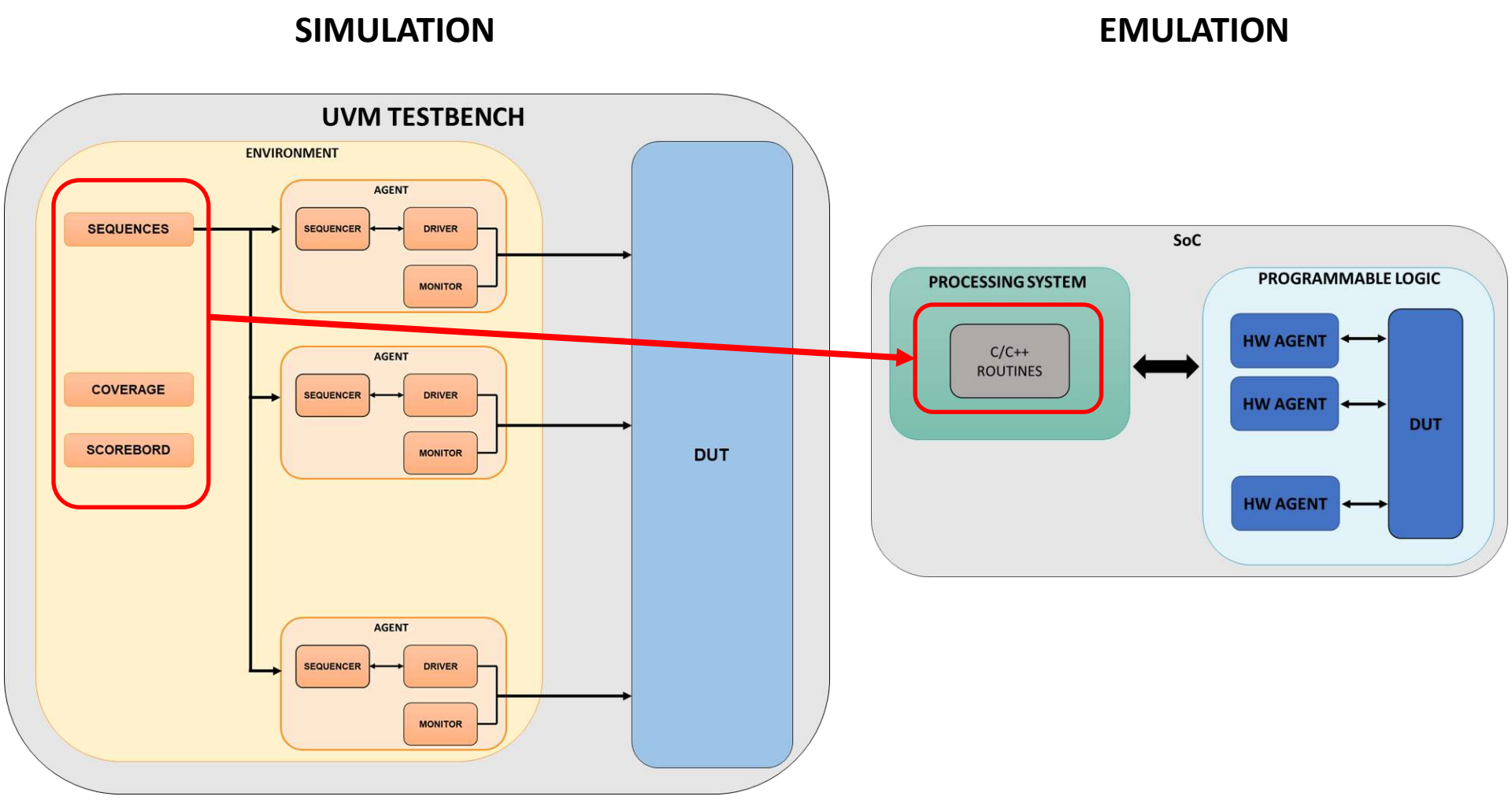

Next Year

- The activities planned for the third PhD year could be divided in two macro activities:
  - Development of ASIC test chip for the hardware accelerator of the Neural Networks
  - Development of an automated tool for both software simulation and hardware emulation of complex SoC

Thanks for the attention !