UNIVERSITÀ DEGLI STUDI DI NAPOLI FEDERICO II

DOTTORATO DI RICERCA / PHD PROGRAM IN
INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

Activities and Publications Report

PhD Student: Giorgio Farina

Student DR number: DR995861

PhD Cycle: XXXVII
PhD Cycle Chairman: Prof. Stefano Russo

PhD program student's start date: 01/11/2021
PhD program student's end date: 31/10/2024

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PhD scholarship funding entity: CINI – Consorzio Interuniversitario Nazionale per l'Informatica

General information

Giorgio Farina received in year 2021 the Master Science degree in Computer Engineering from the University of Napoli Federico II. He attended a curriculum in Computer Engineering within the PhD program in Information Technology and Electrical Engineering. He received a grant from the CINI-Consorzio Interuniversitario Nazionale per l'Informatica.

Study activities

Attended Courses

Year	Course Title	Type	Credits	Lecturer	Organization
1st	Software Security	MSc course	6	Prof. Roberto Natella	University of Napoli Federico II
1st	Real-Time Industrial Systems	MSc course	6	Prof. Marcello Cinque	University of Napoli Federico II
1st	Virtualization technologies and their applications	Ad hoc course	5	Prof. Luigi De Simone	ITEE
1st	Statistical data analysis for science and engineering research	Ad hoc course	4	Prof. Roberto Pietrantuono	ITEE
2nd	IoT Data Analysis	Ad hoc course	4	Prof. Raffaele Della Corte	ITEE

Attended PhD Schools

Year	School title	Location	Credits	Dates	Organization
2nd	Verification and Validation of Automated Systems' Safety and Security	Genova, Italy	6	18/07/2023 (three days)	VALU3S

Attended Seminars

Year	Seminar Title	Credits	Lecturer	Lecturer affiliation	Organization
1st	Challenges towards LargeScale Quantum Computers	0.2	Ing. Vincenzo Maisto	University of Napoli Federico II	University of Napoli Federico II
1st	An Introduction to Deep Learning for Natural Language Processing	0.2	Dr. Marco Valentino	Idiap Research Institute, Martigny, Switzerland- University of Manchester, United Kingdom	ITEE
1st	Explainable Natural	0.2	Dr. Marco	Idiap Research	ITEE

	Language Inference		Valentino	Institute, Martigny, Switzerland- University of Manchester, United Kingdom	
1st	Using Delays For Control	0.4	Prof. Emilia Fridman	Tel Aviv University, Tel Aviv, Israel, School of Electrical Engineering Tel Aviv University	ITEE
2nd	Threat Hunting & Incident Response	0.4	Dr. Artem Artemov	Group-IB	ITEE
2nd	Cybercrime and Information Warfare: National and International Actors	0.4	Dr. Pierluigi Paganini	ENISA	ITEE
2nd	Ricerca e formazione nella società della transizione digitale	1	Prof. Stefano Russo	University of Napoli Federico II	CINI
3rd	Challenges in Resilient Infrastructures, Systems, and Processes	2	Prof. Saurabh Bagchi	University of Purdue	CRISP Workshop, Purdue University
3rd	Resource Efficient Large Scal ML: Plan Before You Run	0.4	Prof. Shivaram Venkataram	University of Wisconsin, Madison	Purdue University
3rd	When Research comes full circle: A missed opportunity and what to learn from it	0.4	Prof. Mike Reiter	Professor Departments of Computer Science and. Electrical & Computer Engineering at Duke University	Purdue University

Research activities

Giorgio Farina participated in research on resilient, dependable, and secure cyber-physical systems, focusing mainly on two key aspects of the emerging real-time cloud paradigm: (I) memory access isolation and (II) failure isolation among execution environments of co-located customers. Regarding memory isolation, he addressed the challenge of evaluating a black-box hardware controller in new Intel server processors. He also provided empirical evidence that memory queue occupancy can detect interference levels, i.e., the number of memory contenders, suggesting a new detection/regulation approach to safeguard the memory bandiwdth of critical tasks without jeopardizing the execution of non-critical tasks. In terms of failure isolation, Giorgio introduced a novel record and replay method to assess hypervisor robustness without manual

effort, focusing on the shared, privileged software layer running across customers. He implemented a proof-of-concept tool called IRIS within the Xen hypervisor.

In addition to real-time cloud scenario, he contributed to build a programmer-friendly confidential execution environment in Android, and he worked also on the assessment of CPU virtualization fault-tolerance mechanisms in cloud platforms and on the log data analysis in train trasnsport systems.

Credits summary

PhD Year	Courses	Seminars	Research	Tutoring / Supplementary Teaching
1st	21	1	35.8	0
2nd	12	1.8	42	0
3rd	0	2.8	64	0

Research periods in institutions abroad and/or in companies

PhD Year	Institution / Company	Hosting tutor	Period	Activities
3rd	University of Purdue, West Lafayette, Indiana, USA	Prof. Saurabh Bagchi	October 27, 2023 - June 27, 2024	I worked on a “programmer-friendly confidential execution environment in Android”

PhD Thesis

In the PhD Thesis, Giorgio Farina focuses on two key aspects of the emerging real-time cloud paradigm: (I) memory access isolation and (II) failure isolation across execution environments of different co-located customers. Regarding memory isolation, he addressed the challenge of evaluating a black-box hardware controller (Memory Bandwidth Allocation) in new Intel server processors by developing a workload capable of bypassing the regulation shown by generic state-of-the-art workloads by over 50%, warning the community about the risks of adopting generic workloads for specialized controllers. He also provided empirical evidence that memory queue occupancy can detect interference levels, i.e., the number of memory contenders, within one-sixth of the regulation period. In terms of failure isolation, he introduced a novel record and replay method to assess hypervisor robustness without manual effort, focusing on the shared, privileged software layer running across customers. He implemented a proof-of-concept tool called IRIS within the Xen hypervisor. The results demonstrated that IRIS could generate new test cases, reaching valid hypervisor states with significant time improvements (from 42.5% to 99.6%) and high accuracy, with code coverage fitting between 92.1% and 100% compared to the recorded execution.

Research products

Research results appear in *1* paper published in international journals, *6* contributions to international conferences.

List of scientific publications

International journal papers

1) Giorgio Farina, Gautam Gala, Marcello Cinque, Gerhard Fohler
Enabling memory access isolation in real-time cloud systems using Intel's detection/regulation capabilities,
International Journal of Systems Architecture
Volume 137, April 2023, 102848, DOI: 10.1016/j.sysarc.2023.102848

International conference papers

1) Giorgio Farina, Gautam Gala, Marcello Cinque, Gerhard Fohler,
Assessing Intel's Memory Bandwidth Allocation for resource limitation in real-time systems,
IEEE 25th International Symposium On Real-Time Distributed Computing (ISORC),
Västerås, Sweden, 17-18 May 2022, IEEE, DOI: 10.1109/ISORC52572.2022.9812757

2) Carmine Cesarano; Marcello Cinque; Domenico Cotroneo; Luigi De Simone; Giorgio Farina
IRIS: a Record and Replay Framework to Enable Hardware-assisted Virtualization Fuzzing,
2023 53rd Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN),
Porto, Portugal, 27-30 June 2023, IEEE, DOI: 10.1109/DSN58367.2023.00045

3) Marco Barletta, Marcello Cinque, Luigi De Simone, Raffaele Della Corte, Giorgio Farina, Daniele Ottaviano
RunPHI: Enabling Mixed-criticality Containers via Partitioning Hypervisors in Industry 4.0,
2022 IEEE International Symposium on Software Reliability Engineering Workshops (ISSREW),
Charlotte, NC, USA, p. 134-135, 26 December 2022, IEEE, DOI: 10.1109/ISSREW55968.2022.00058

4) Marco Barletta, Marcello Cinque, Luigi De Simone, Raffaele Della Corte, Giorgio Farina, Daniele Ottaviano
Partitioned Containers: Towards Safe Clouds for Industrial Applications,
2023 53rd Annual IEEE/IFIP International Conference on Dependable Systems and Networks-Supplemental Volume (DSN-S),
Porto, Portugal, p. 84-88, June 2023, IEEE, DOI: 10.1109/DSN-S58398.2023.00029

5) Marcello Cinque, Raffaele Della Corte, Giorgio Farina, Stefano Rosiello
An unsupervised approach to discover filtering rules from diagnostic logs,
2022 IEEE International Symposium on Software Reliability Engineering Workshops (ISSREW),
Charlotte, NC, USA, p. 1-6, 26 December 2022, IEEE, DOI: 10.1109/ISSREW55968.2022.00030

6) Marcello Cinque, Raffaele Della Corte, Giorgio Farina, Stefano Rosiello
AID4TRAIN: Artificial Intelligence-Based Diagnostics for TRAins and INdustry 4.0,
European Dependable Computing Conference 2022 Workshops,
Zaragoza, Spain, vol 1656, p. 1-6, 05 September 2022, Springer, Cham, DOI: 10.1007/978-3-031-16245-9_7

Awards and Prizes

Best Industry Paper Award ISSRE 2022 for the paper: "An unsupervised approach to discover filtering rules from diagnostic logs "

Date 15/10/2024

PhD student signature

Supervisor signature